Lecture 05.01   Analyzing a full-wave bridge rectifier

In Lab Exercise 05, we will build and measure the response of a diode full-wave bridge rectifier circuit. This lecture is intended to introduce this circuit, used to convert AC signals to DC signals.

Figure 05.1 shows a circuit diagram for a full-wave bridge rectifier. Four diodes perform the rectification. A capacitor in parallel with the load effectively smooths this rectified signal.

There are four diodes, so there are $4^2 = 16$ possible diode states! We'll try to make good guesses and avoid invalid states in our analysis.

05.01.1   Analyzing the circuit

Let's begin by thinking about our diode model. Piecewise linear is our go-to. However, we can simplify it even further if we assume the load won't draw much current. The load in Lab Exercise 05 is 1 kΩ—so only small currents will flow through these diodes. We could go through the process of determining the current flow and choosing an operating point for diode resistances, but with such small current flow, we'd still be stuck setting all $R_d = 0$.

So we choose to model the circuit as shown in Figure 05.2. At this point we could perform a single analysis for the entirety of the circuit, but with the number of diodes, this gets messy. Therefore, we choose to reason our way through the potential states and analyze the few that survive.

Consider the case of $V_S > 0$. The only potential pathway for current is through D_1 and returning through D_2. It cannot return through D_4, since its
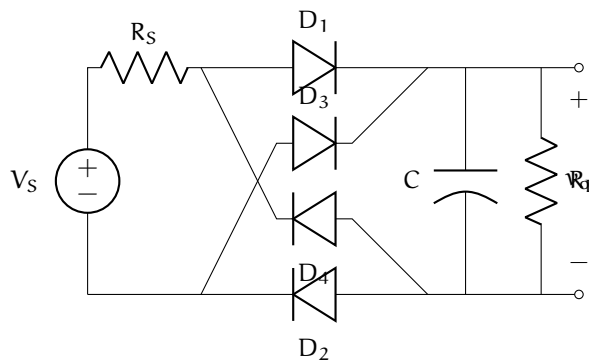

Figure 05.1: full wave bridge rectifier circuit, including a source output resistance R_S.
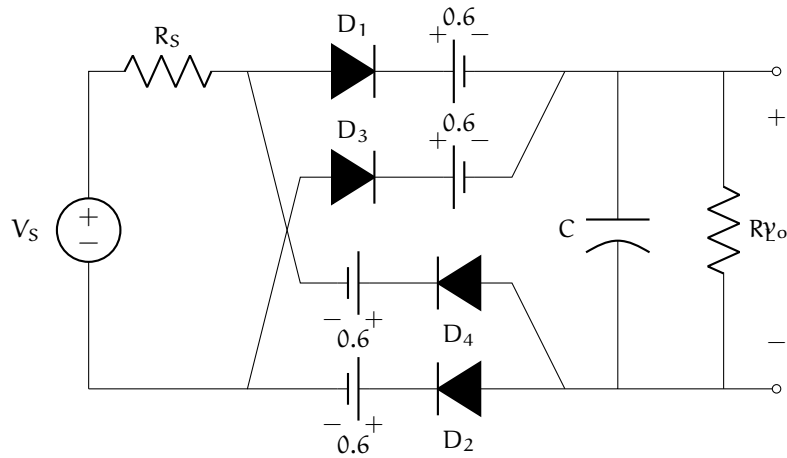
Figure 05.2: full wave bridge rectifier circuit, including a source output resistance R_S.

voltage drop will be negative. Similarly, current cannot flow from ground, through D_3, to the positive side of the capacitor. That is, D_1 and D_3 cannot both be in forward-bias and neither can D_2 and D_4. A similar consideration of $V_S \leqslant 0$ shows that current can only flow to the load via D_3 and return through D_4.

Furthermore, we cannot have current flow to the load side of the circuit and not return, so we can eliminate any such cases. This leaves only three possible states.

primary charge state S_1 When D_1 is ON, current must return via D_2, so it must also be ON. D_3 and D_4 are off, corresponding to Figure 05.3. So, using bold face for ON:

$$S_1 = \left\{ \ \mathbf{D_1}, \quad \mathbf{D_2}, \quad D_3, \quad D_4 \ \right\}. \tag{05.1}$$

secondary charge state S_2 When D_3 is ON, current must return via D_4, so it must also be ON. D_1 and D_2 are off, corresponding to Figure 05.4. So, using bold face for ON:

$$S_2 = \left\{ \ D_1, \quad D_2, \quad \mathbf{D_3}, \quad \mathbf{D_4} \ \right\}. \tag{05.2}$$

discharge state S_3 When all four diodes are OFF, the charged capacitor discharges into R_L, corresponding to Figure 05.5. So our discharge state is:

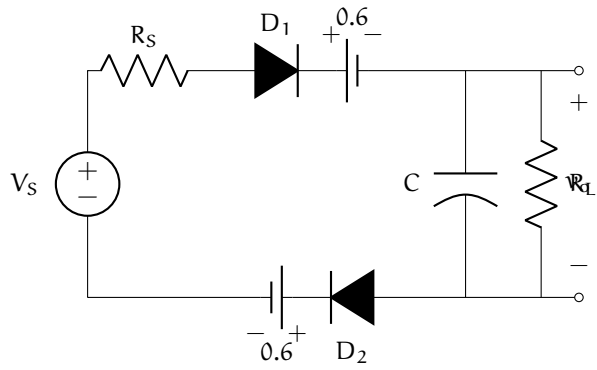$$S_3 = \left\{ \ D_1, \quad D_2, \quad D_3, \quad D_4 \ \right\}. \tag{05.3}$$

Figure 05.3: the primary charge state S_1 ($V_S > 1.2 + v_o$), in which only D_1 and D_2 are in forward-bias.
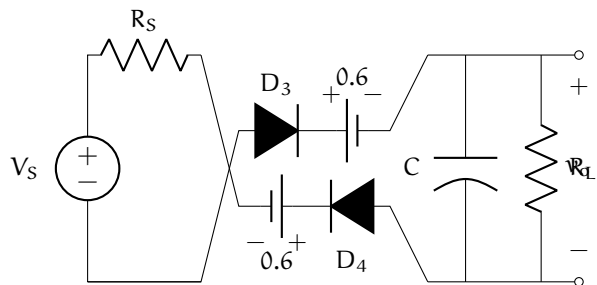
Figure 05.4: the secondary charge state S_2 ($V_S < -1.2 + v_o$), in which only D_3 and D_4 are in forward-bias.
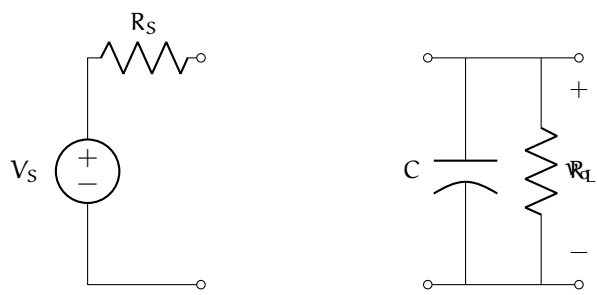
Figure 05.5: the discharge state S_3 ($-1.2 + v_o < V_S < 1.2 - v_o$), in which all diodes are in reverse-bias.

Let's consider each of these states as they arise from the initial time. As we do so, we can examine both the conditions that give rise to each diode state S_1–S_3 and how the circuit behaves during each state.

Let's assume the capacitor begins uncharged. This isn't much of a stretch, considering that it has a load resistor to which it can discharge.

Let's also assume V_S increases sinusoidally from 0 V. At first, there's not enough voltage drop across D_1 to turn it on, so we're stuck in the discharge state S_3 until V_S increases enough to overcome both the 0.6 V associated with D_1 and the 0.6 V associated with the return diode D_2—so when $V_S > 1.2$. At that point, we transition to S_1.

As V_S continues to rise, $v_o = v_C = v_{R_L}$ increases—that is, the capacitor charges. When V_S decreases, the capacitor voltage doesn't immediately disappear, since its discharge into R_L is typically relatively slow. As the decrease in V_S continues, it will switch back to state S_3, but this time before reaching 1.2 V because now *the capacitor is still charged* (although it is slowly discharging). Reconsidering the S_3, we see that $V_S > 1.2 + v_o$ for the diodes to be on. So we have now discovered that an alternative formulation for S_1:

$$S_1 = \{V_S > 1.2 + v_o\}. \tag{05.4}$$

Let's consider development of output voltage during S_1. In this state, we can analyze the circuit as follows. Here are the elemental equations.

$$
\begin{array}{c|c}
C & \dfrac{dv_C}{dt} = \dfrac{1}{C} i_C \\[2ex]
R_S & v_{R_S} = i_{R_S} R_S \\[2ex]
R_L & v_{R_L} = i_{R_L} R_L
\end{array}
$$

Similarly, KCL and KVL give the following equations.

$$
\begin{array}{c|c}
\text{KCL} & i_{R_S} = i_C + i_{R_L} \\[2ex]
\text{KVL}_1 & V_S = v_{R_S} + v_C \\[2ex]
\text{KVL}_2 & v_C = v_{R_L}
\end{array}
$$

Let's reduce this to a differential equation in v_C, starting with the capacitor

elemental equation:

$$\frac{dv_C}{dt} = \frac{1}{C}(i_{R_S} - i_{R_L}) \tag{KCL}$$

$$= \frac{1}{C}\left(\frac{v_{R_S}}{R_S} - \frac{v_{R_L}}{R_L}\right) \tag{resistors}$$

$$= \frac{1}{C}\left(\frac{V_S - v_C}{R_S} - \frac{v_C}{R_L}\right) \Rightarrow \tag{KVL$_{1,2}$}$$

$$\tau\frac{dv_C}{dt} + v_C = \frac{1}{R_S C}V_S \tag{05.5}$$

where

$$\tau = \frac{R_S R_L}{R_S + R_L}C. \tag{05.6}$$

Word. The solution to this familiar differential equation for initial capacitor voltage $v_{C0} = v_C(t)|_{t=t_0}$ and input $V_S(t) = A\sin(\omega t)$ is our output $v_o(t)$.

The other charging state S_2 is similar and yields the alternative formulation of S_2:

$$S_2 = \{V_S < 1.2 - v_o\}. \tag{05.7}$$

The discharging state S_3 is the easiest circuit to analyze: it is simply the capacitor C with an initial voltage discharging through the load R_L, with no forcing.

Due to the nonlinearities, cycles through the states may be required before settling into a steady state. This relatively complicated analysis is sometimes bypassed by the method that follows in 05.01.2.

05.01.2   A quick-and-dirty model

A full time-domain analysis of the circuit is preferable to this quick-and-dirty model, but this method is a nice way to quickly estimate the results.

The DC component of a signal is its average value. The average value of the signal across the load can be predicted if we know the maximum value of the rectified signal (sans capacitor) A_r and the ripple voltage Δv_o, which is the steady state voltage from the high-to-low output voltage. The maximum value of the rectified signal should be

$$A_r = A - 2 \cdot 0.6,$$

where A is the input amplitude and the 0.6 V term comes from the voltage drop across a diode. Then the DC component of the signal should be approximately

$$v_{DC} = A_r - \frac{\Delta v_o}{2}.$$

If we assume the ripple voltage Δv_o is relatively small and the AC signal has a high-enough frequency that it changes faster than the capacitor, we can assume that the full wave rectifier's output can be approximated by the expression

$$\Delta v_o = \frac{i_{R_L}}{2fC} \tag{05.8}$$

where f is the input signal frequency.

How do we know the load current i_{R_L} if we don't do the entire circuit analysis? It turns out that most loads for AC-to-DC conversions are actually voltage regulators, which draw steady currents. In the case of a resistor load, we can use a conservative estimate: the max $v_{DC} = A_r$ (no ripple), so from Ohm's law the max $i_{R_L} = v_{DC}/R_L$. Using the max i_{R_L} in `Equation 05.8` yields the max ripple.[1]

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[1]This reasoning may appear circular: did we not assume the ripple was zero, then derive from that its maximum? In fact, we *dropped* the assumption that the ripple was zero once we derived the maximum current. This is an example of a *bootstrapping method*. We could actually iterate on this to get a better and better approximations, re-using better and better approximations of v_{DC} for better i_{R_L} for better Δv_o for better v_{DC}, etc.